Jerry Zhao

Telephone: (215) 237-7703 *Email*: jzh@berkeley.edu *Github*: github.com/jerryz123

Education

In progress: Ph.D. in Computer Science **2019 -**
University of California, Berkeley
Advisor: Krste Asanović

B.S. Electrical Engineering and Computer Science **2015 - 2019**
University of California, Berkeley **GPA: 3.98**
Dean's Honors, EE/CS Departmental Honors, Tau Beta Pi, Eta Kappa Nu

Experience

Graduate/Undergraduate Student Researcher - The ASPIRE/ADEPT Lab August 2016 - Present

- Core microarchitect of the SonicBOOM (Berkeley Out-of-Order Machine) project.
- Core developer of the Chipyard hardware design framework.
- Developed various software tools for running state-of-the-art neural networks on research hardware accelerators

Undergraduate Student Researcher - Berkeley AUTOLAB August 2017 - August 2018

- Developed FLUIDS, a lightweight Python urban driving simulator for prototyping novel autonomous driving system

Performance Infrastcture Intern - NVIDIA May 2017 - August 2017

- Developed tool for remote profiling and monitoring of GPU clusters

Research and Development Intern - Sandia National Laboratories June 2016 - August 2016

- Contributed to the development of metrics for cybersecurity risk analysis

Projects

SonicBOOM 2018 - Ongoing

- Core microarchitect of SonicBOOM, the highest-IPC open-source RISC-V out-of-order core
- Implemented instruction-fetch and branch-prediction pipelines. Added new support for variable-width instructions. Developed novel composable branch predictor generator, and implemented state-of-the-art TAGE hardware branch predictor
- Implemented superscalar load-store-unit, with out-of-order superscalar issue to a banked L1 data-cache. Added new L1 line-buffers and hardware next-line-prefetcher
- Prototyped mitigation for Spectre-like side-channel attacks. Implemented lazy-write line-buffers to hide speculative accesses from potential attackers
- Prototyped out-of-order vector-execution pipeline for early version of the RISC-V vector specification

Chipyard 2019 - Ongoing

- Core developer of Chipyard, an open-source SoC design, evaluation, and implementation framework
- Unified target/harness RTL generators across various SW-simulation, FPGA-emulation, and VLSI flows
- Currently redesigning clock/reset distribution to be amenable for various use-cases, including multi-clock

ONNX-Halide 2019

- Developed transpiler to convert ONNX-formatted neural network models to the Halide image-processing DSL
- Automated deployment of standard ONNX models on research hardware with Halide support

FLUIDS 2018

- Developed lightweight Python urban driving simulator for prototyping novel autonomous driving systems

Miscellaneous

Skills: Chisel, Scala, Python, C, C++, git, GNU tools, Linux
Interests: SoC design, microarchitecture, accelerator systems integration, hardware-software codesign